CLAIMS:

1. A method of performing an IDDQ test of an electronic circuit, the method comprising

- using a power supply unit to supply power supply current to the electronic circuit;
- adjusting an output impedance of the power supply unit to a value selected for the electronic circuit, the value having been selected so that a resonance circuit that comprises a connection between the power supply unit and the electronic circuit is substantially critically dampened;
- measuring IDDQ current with a current sensing element that senses a value of the current supplied to the electronic circuit between an external power supply source and the power supply regulating circuit that supplies power to the electronic circuit under test, outside a part of the power supply unit that affects the output impedance.

2. A method according to Claim 1, wherein said power supply unit contains a regulating loop, for regulating a supply voltage applied to the electronic circuit at least during measurement of the IDDQ current, said measuring being performed on an incoming supply current that the power supply unit draws to provide the regulated voltage to the electronic circuit.

3. A method according to Claim 1, wherein a further incoming supply current is supplied to the power supply unit in parallel with said incoming supply current, the method comprising regulating the further incoming supply current to a level equal to a consumed current that is consumed by the power supply unit.

4. An IDDQ test system, comprising

- an electronic circuit under test;
- a power supply unit, with a power supply output coupled to the electronic circuit under test, the power supply unit comprising a regulating loop for regulating a power supply voltage applied to the electronic circuit under test, the power supply unit having a current input for receiving an incoming supply current that the supply unit draws to supply the power supply voltage;

- a current sense element arranged to measure at least part of the incoming supply current and to generate an IDDQ error signal dependent on a level of said part of the incoming supply current.

5. An IDDQ test system according to Claim 4, comprising
- a first current source coupled to the current input of the power supply unit in parallel with the current sense element; and
- an adjustment circuit arranged to adjust a further part of the incoming supply current that is supplied by the first current source to a level of consumed current that is consumed by the power supply unit.

6. An IDDQ test system according to Claim 4, wherein the power supply unit comprises
- a transistor with a control input and having a main current channel coupled between the current input and an output that is coupled to the electronic circuit under test;
- a programmable current source coupled to the output so as to substantially set a quiescent through the main current channel of the transistor to a programmable value;
- a feedback circuit coupled between the output and the control input of the transistor, so as to regulate a voltage at the output with the transistor in source follower or emitter follower operation.

7. An IDDQ test system according to Claim 4, wherein the power supply unit comprises
- a common reference connection, the electronic circuit under test conducting quiescent power supply current form the output of the power supply unit to the common reference connection, the current sense element being coupled between the current input and the common reference connection;
- a series arrangement of a first and second power supply that float with respect to the common reference connection at least for part of the time, the power supply unit being fed from terminals of said series arrangement;
- a further current source coupled to the current input of the power supply unit in parallel with the current sense element, the first current source drawing current from one of the terminals of the series arrangement;

- a current control circuit, comprising a current path from a node between the first and second power supplies and the common reference connection, the current control circuit having an output coupled to a control input of the further current source, the current control circuit being arranged to regulate the current through the further current source so that substantially no current flows through the current path.

8. An IDDQ test system according to Claim 4, wherein the power supply unit comprises

- a further current source coupled to the current input of the power supply unit in parallel with the current sense element, the first current source drawing current from one of the terminals of the series arrangement;
- a current control circuit, the current control circuit having an output coupled to a control input of the further current source, the current control circuit being arranged to regulate the current through the further current source so that substantially no current flows through current sense element during a calibration phase when the electronic circuit under test is decoupled from the output of the power supply unit.

9. An IDDQ test apparatus, comprising

- a power supply output for connecting an electronic circuit under test;
- a power supply unit, with a power supply output coupled to the power supply output, the power supply unit comprising a regulating loop for regulating a power supply voltage applied to the electronic circuit under test, the power supply unit having a current input for receiving an incoming supply current that the supply unit draws to supply the power supply voltage;
- a current sense element arranged to measure at least part of the incoming supply current and to generate an IDDQ error signal dependent on a level of said part of the incoming supply current.